

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

- 31 1. (Currently Amended) A microcomputer having an on-chip debugging function, comprising:
- a central processing unit for executing instructions; and
- a first monitor ~~means for performing~~ section which performs data transfer to and from a second monitor ~~means section, determining~~ determines a primitive command to be executed based on the receive data from said second monitor ~~means section~~, and ~~performing~~ performs processing for execution of the determined primitive command, said second monitor ~~means section~~ being provided outside said microcomputer and for performing a processing to convert a debugging command into at least one primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section.
2. (Currently Amended) The microcomputer according to claim 1, ~~wherein~~ said primitive command includes a command for starting an execution of a user program, a command for writing data to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.
123. (Currently Amended) The microcomputer according to claim 1, ~~further comprising~~ the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.
34. (Currently Amended) The microcomputer according to claim 2, ~~further comprising~~ the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on the memory map in the debugging mode.

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5. (Currently Amended) The microcomputer according to claim 1, further comprising the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

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6. (Currently Amended) The microcomputer according to claim 2, further comprising the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on the memory map in the debugging mode.

16 7. (Currently Amended) The microcomputer according to claim 1, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor means section,

—wherein, on condition that said first monitor means section being a slave has received data from said second monitor means section being a master, said first monitor means section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor means section.

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8. (Currently Amended) The microcomputer according to claim 2, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor means section,

—wherein, on condition that said first monitor means section being a slave has received data from said second monitor means section being a master, said first monitor means section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor means section.

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9. (Currently Amended) The microcomputer according to claim 1, wherein the data received from said second monitor ~~means~~ section includes an identification data of the primitive command to be executed by said first monitor ~~means~~ section.

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10. (Currently Amended) The microcomputer according to claim 2, wherein the data received from said second monitor ~~means~~ section includes an identification data of the primitive command to be executed by said first monitor ~~means~~ section.

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11. (Currently Amended) The microcomputer according to claim 1, wherein said first monitor ~~means~~ section transfers fixed-length data to and from said second monitor ~~means~~ section.

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12. (Currently Amended) The microcomputer according to claim 2, wherein said first monitor ~~means~~ section transfers fixed-length data to and from said second monitor ~~means~~ section.

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13. (Currently Amended) The microcomputer according to claim 1, wherein a monitor program for executing a processing of said first monitor ~~means~~ section is stored in a ROM.

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14. (Currently Amended) The microcomputer according to claim 2, wherein a monitor program for executing a processing of said first monitor ~~means~~ section is stored in a ROM.

15. (Currently Amended) The microcomputer according to claim 1,
— wherein said first monitor ~~means~~ comprises section includes:
a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and
a circuit for sending and receiving data based on said first sampling clock, and

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 wherein said first monitor-means section supplies said first clock to said second monitor-means section as a signal for causing a second frequency division circuit included in said second monitor-means section to generate a second sampling clock.

16. ⁹ (Currently Amended) The microcomputer according to claim 2,

— wherein said first monitor means comprises section includes:

a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and

wherein said first monitor-means section supplies said first clock to said second monitor-means section as a signal for causing a second frequency division circuit included in said second monitor-means section to generate a second sampling clock.

17. ²⁴ (Currently Amended) The microcomputer according to claim 1, wherein:

— said first monitor-means section includes a monitor RAM which is readable and writable, and

— when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor-means section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

18. ¹⁰ (Currently Amended) The microcomputer according to claim 2, wherein:

said first monitor-means section includes a monitor RAM which is readable and writable, and

— when a break of an execution of an user program occurs and a mode is shifted to a debugging mode, said first monitor-means section saves a program counter value of said central processing unit and contents of an internal register into said monitor RAM.

19. ²⁶ (Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 1;

an input source of data to be processed by said microcomputer;

and

an output device for outputting data processed by said microcomputer.

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(Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim 2;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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(Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim ¹²~~3~~;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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(Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim ¹⁴~~5~~;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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(Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim ¹⁶~~7~~;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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(Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim ¹⁸~~9~~;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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(Currently Amended) An electronic instrument, comprising:

a microcomputer according to claim ²⁰~~11~~;

an input source of data to be processed by said microcomputer; and

an output device for outputting data processed by said microcomputer.

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26. (Currently Amended) An electronic instrument, comprising:
a microcomputer according to claim ²²13;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

27. (Currently Amended) An electronic instrument, comprising:
a microcomputer according to claim 18;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

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28. (Currently Amended) An electronic instrument, comprising:
a microcomputer according to claim ²⁴17;
an input source of data to be processed by said microcomputer; and
an output device for outputting data processed by said microcomputer.

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29. (Currently Amended) A debugging system for a target system including a microcomputer, said debugging system comprising:

a second monitor means for performing section which performs processing for converting a debugging command issued by a host system into at least one primitive command; and

a first monitor means for performing section which performs data transfer to and from said second monitor means section, determining determines a primitive command to be executed based on the receive data from said second monitor means section, and performing performs processing for execution of the determined primitive command, wherein the second monitor section converts the debugging command into the primitive command in order to reduce the size of an instruction code for realizing the first monitor section or a scale of the first monitor section.

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(New) The debugging system according to claim ²⁸29, said primitive command includes a command for starting an execution of a user program, a command for writing data

to an address on a memory map in a debugging mode and a command for reading data from the address on said memory map.

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31. (New) The debugging system according to claim ²⁸29, the first monitor section includes a control register used for execution of instructions in said central processing unit and having an address thereof allocated on a memory map in a debugging mode.

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32. (New) The debugging system according to claim ²⁸29, the first monitor section includes a monitor RAM into which contents of an internal register of said central processing unit are saved, and having an address thereof allocated on a memory map in a debugging mode.

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33. (New) The debugging system according to claim ²⁸29, further comprising a terminal connected to a single bidirectional communication line for performing a half-duplex bidirectional communication between said terminal and said second monitor section, wherein, on condition that said first monitor section being a slave has received data from said second monitor section being a master, said first monitor section performs a processing corresponding to the received data and sends response data corresponding to the received data to said second monitor section.

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34. (New) The debugging system according to claim ²⁸29, the data received from said second monitor section includes an identification data of the primitive command to be executed by said first monitor section.

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35. (New) The debugging system according to claim ²⁸29, wherein said first monitor section transfers fixed-length data to and from said second monitor section.

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36. (New) The debugging system according to claim ²⁸29, wherein a monitor program for executing a processing of said first monitor section is stored in a ROM.

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37. (New) The debugging system according to claim ²⁸29, said first monitor section includes:

B1 a first frequency division circuit for dividing a first clock and for generating a first sampling clock for sampling each bit in data sent and received according to start-stop synchronization; and

a circuit for sending and receiving data based on said first sampling clock, and wherein said first monitor section supplies said first clock to said second monitor section as a signal for causing a second frequency division circuit included in said second monitor section to generate a second sampling clock.